

KPR Institute of Engineering and Technology

(Autonomous, NAAC "A")

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NBA Accredited (CSE, ECE, EEE, MECH, CIVIL)

| LAYOUT AND ANALYSIS OF CMOS CIRCUITS USING SYMICA TOOL |   |  |  |  |
|--|---|--|--|--|
| Event No   | EC050   |  |  |  |
| Organizing Department                                  | Electronics and Communication Engineering   |  |  |  |
| Associate Dept.   NSC                                  | Institution of Electronics and Telecommunication Engineering<br>International Society for Technology in Education |  |  |  |
| Date   | 14/03/2023  |  |  |  |
| Time   | 02:00 PM to 04:00 PM  |  |  |  |
| Event Type   | Expert Talk   |  |  |  |
| Event Level  | Dept. Level   |  |  |  |
| Venue  | Thanam Hall   |  |  |  |
| Meeting Medium   |   |  |  |  |
| Meeting Link   | https://meet.google.com/dtj-qros-vve  |  |  |  |







## **Resource Persons**

| SI | Туре               | Name       | Designation                    | Company              | Email                  | Phone     |
|----|--------------------|------------|--------------------------------|----------------------|------------------------|-----------|
| 1  | Resource<br>Person | Amit Saini | Director and<br>Technical Head | Cadre Design Systems | amit@cadredesign.co.in | xxxxxxxxx |

## **Involved Staffs**

| SI | Name           | Role        |
|----|----------------|-------------|
| 1  | Kathirvelu M   | Coordinator |
| 2  | Arun Sekar R   | Coordinator |
| 3  | Muralidharan J | Coordinator |

## Outcome

Symica Design Environment integrates all the tools necessary for circuit design and simulation using library manager, schematic editor, symbol editor, hierarchy editor, simulation environment, input/output translators, etc. It also allows the user to manage the operation of the various components. The design environment also facilitates the preparation and execution of simulations and the inspection and interpretation of simulation results. The students can able to design the CMOS circuits using Symica tool and analyze and validate the performance parameters.

## **Event Summary**

The online webinar started with the welcome note by Dr. R Arun sekar, following the welcome address, a brief information regarding the Symica tool was explained by Amit Saini, Director and Techical Head of Cadre design systems. Later he delivers a comprehensive set of EDA tools that enable companies around the world to design analog and mixed-signal integrated circuits with full flow. Further, he explained the major capabilities of modern IC development suites. Easy accommodation of different Process Development Kits (PDK) as well as affordable and flexible pricing that makes Symica an attractive solution for startups/Academic Institutes and independent researchers. He explained the major capabilities of modern IC development suites. Easy accommodation of different Process Development Kits (PDK) as well as affordable pricing makes that Symica an attractive solution for startups and independent researchers. Mid-size and well-established semiconductor companies can and Symica is a cost-saving solution for expanding their design forces in addition to limit license sets from major EDA vendors. Moreover, Complete solution for analog and mixed-signal IC designer is explained by him. Then narrated about the Accurate circuit simulation, Analog, behavioral and digital mixed-mode simulation. Industry compatible: easy import-export of entire design.



Silicon proven Competitive and fexible pricing. He also explored the SymSpice which is an original SPICE circuit simulator completely developed by the Symica R&D team. SymSpice provides simulation speed and accuracy at the "golden" SPICE level. SymSpice supports all commonly used transistor models and is compatible with industry-standard netlist formats.

Finally, he demonstrated the SymSpice Turbo specially designed to work with very large scale integrated circuits and system on chips. In recent years several Fast-Spice tools have appeared on the market and they trade speed for accuracy. Symica's proprietary math methods provide accurate Fast-Spice simulation maintaining accuracy at "golden" SPICE level. Simulation time reduction factor is highly dependent on the type of design and in "typical" designs involving several thousand transistors it is about 3 to 10 and in an exceptional case we can find a factor up to 1,000. At the end, all the coordinators talked the resourse person for his valuable inputs.



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